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[Claim(s)]

[Claim 1] The electric charge read-out part which has-dimensional [1] or two-dimensional arrangement is formed in the surface of the semiconductor thin board which has the 1st conducted type of current. In the semiconductor energy detector which detects the energy of the electromagnetic waves which enter from the back to the formation side of said electric charge read-out part of said semiconductor thin board, or a charged particle The semiconductor layer which consists of a semiconducting material which has a bigger band gap than the band gap which has the 1st conducted type of current, and the composition material of a semiconductor thin board has is formed in the back of said semiconductor thin board. It is the semiconductor energy detector characterized by said semiconductor thin board and said semiconductor layer carrying out hetero combination.

[Claim 2] The formation material of said semiconductor thin board and the formation material of said semiconductor layer are semiconductor energy detectors according to claim 1 characterized by what it is a material of the same kind, and the crystal structure is [the thing] different.

[Claim 3] The formation material of said semiconductor thin board and the formation material of said semiconductor layer are semiconductor energy detectors according to claim 1 characterized by what is been a material of a different kind.

[Claim 4] It is the semiconductor energy detector according to claim 1 characterized by what photoelectrical conversion is formed in the thickness which is not performed substantially for inside said semiconductor layer.

[Claim 5] The 1st process which forms the electric charge read-out part which has-dimensional [1] or two-dimensional arrangement in the surface of the semiconductor board which has the 1st conducted type of current, The back of said semiconductor board to the formation side of said electric charge read-out part is processed. [said semiconductor board / the 2nd process used as a semiconductor thin board, and the back of said semiconductor thin board] The 3rd process which deposits the semiconducting material which carries out a hetero-junction to the composition material of said semiconductor thin board, and forms a semiconductor layer while having a bigger band gap than the band gap which has the 1st conducted type of current, and the composition material of a semiconductor thin board has, ****** -- the manufacture method of the semiconductor energy detector characterized by things.

[Claim 6] Formation of the semiconductor layer in said 3rd process is the manufacture method of the semiconductor energy detector according to claim 5 characterized by the thing by a CVD method.

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to an effective back irradiation type electric charge transmission type semiconductor energy detector to irradiation of the energy line whose absorption indices, such as ultraviolet rays, and a gamma ray or a charged particle beam, are very large.
[0002]
[Description of the Prior Art] If an electric charge transmission element (CCD) sends an analog electric charge group to one way in order at the speed which synchronized with the clock pulse from the exterior and the output part is prepared in the end, it will be the very skillful functional device which can change space information into a time series signal. However, in order to take out two-dimensional picture information as a time series signal, the constitutional device of a device is required. If the electric charge was transmitted irradiating light at the above-mentioned device, the electric charge by which light excitation was carried out at each place, and the transmitted electric charge are mixed, the phenomenon called what is called a smear occurs, and a picture signal deteriorates. In order to avoid this, what is called time sharing operation that divides in time time (electric charge transmission period) to transmit the period (electric charge accumulation period) which is irradiating light, and an electric charge can be considered. In this case, the time when a picture signal is outputted is restricted within the transmission time of an electric charge, and a picture signal turns into an intermittent signal.
[0003] Generally, as a practical CCD image pick-up device, a Mikata style of frame transmission (FT) full frame transmission (FFT) and interline transmission (IT) composition is typical, among these a full frame transmission mode is mainly used as an object for Measurement Division.
[0004] A full frame transmission mode is explained hereafter. Drawing 10 and 11 show the composition of a full frame transmission mode, drawing 10 is the upper surface figure, and drawing 11 is the sectional view of the important section. As shown in drawing 10 , by this method, the channel of electric charge transmission is perpendicularly divided by the channel stop diffusion zone 1 formed in the substrate, and forms the pixel sequence corresponding to the number of level pixels by it. On the other hand, it intersected perpendicularly with this channel stop diffusion zone 1, and the transmission electrode group 2 is arranged. Although used by the above-mentioned FT method as a CCD in which the grouping of this electrode group is carried out to two upper and lower sides, CCD for light-receiving is accumulated for an upper half, and it accumulates a signal electric charge for a lower half temporarily, there is no accumulation part at the full frame transmission mode CCD shown in this figure. Therefore, you have to make it light not have to enter into CCD by closing a shutter during time, i.e., read-out time, to transmit an electric charge. In addition, three overflow drains 5 are formed between four-row vertical pixel sequences.
[0005] As shown in drawing 11 , stroke matter serves as area surrounded by the electrode 20 and the channel stop diffusion zone 1 of the number corresponding to the source resultant pulse number (4) of the clock pulse (phi 1 - phi4) which constitutes one step of CCD. The perpendicular transmission clock pulse electrode groups 2 are clock pulses phi1-phi4. The polysilicon electrode 20 is supplied. The interlayer insulation film 19 by PSG (phosphorus glass) is deposited on the upper surface of the polysilicon electrode 20, and gate oxide 21 intervenes between this electrode 20 and n-WERU 22 on the silicon substrate 48.

[0006] When light enters into a light-receiving field, the signal electric charge excited as shown in drawing 11 is one transmission electrode (accumulation electrode) phi 1, i.e., the clock pulse which rose. It is brought together in the potential well 3 under the added polysilicon electrode 20.

[0007] The clock voltage phi 1 - phi4 which were given to the perpendicular transmission electrode group 2 on a light-receiving field after the electric charge accumulation time changed into a signal electric charge finished the lightwave signal It rises one by one and read-out of a signal electric charge is started. However, in the full frame transmission CCD, there is nothing that is called what is called an accumulation part other than a light sensing portion like FT-CCD as having mentioned above. For this reason, if a shutter is closed and the input of a lightwave signal is not intercepted before starting signal read-out, a lightwave signal will newly mix in the signal in the middle of having transmitted, and signal purity falls. However, since it is thought that there is no optical input new during transmission of a signal electric charge when catching a single-engined phenomenon, a shutter etc. is unnecessary.

[0008] Here, signal read-out operation is explained using drawing 10 . A signal electric charge is the pulse phi 1 - phi4 which are given to the clock pulse electrode group 2 for perpendicular transmission. One line is sent at a time below, and it is transmitted to an outgoing end through the level read-out register 6. That is, in this figure, the signal electric charge which is in the bottom line first is simultaneously sent into the level read-out register 6, and it is the clock phi 5 of horizontally high frequency, and phi 6. It is transmitted and is read from an outgoing end as a time series signal. In addition, the level transfer clock phi 5 and phi 6 It is added from the clock pulse electrode group 7 for level transmission. Since the following signal electric charge has already moved to the one-step lower part of a perpendicular register at this time, it goes into the level read-out register 6 by the following perpendicular transmission clock pulse, and is read to an outgoing end. Thus, if the signal electric charge for one screen is altogether read through the level read-out register 6, a shutter will be opened and new signal accumulation operation will be started. As mentioned above, since it operates at high speed compared with a perpendicular register, the level read-out registers 6 are 2 ** clock pulse phi 5 and phi 6. It carries out and fast transmission is made possible.

[0009] Here, the example by which the on-chip was carried out and which reads and expresses an impression clock pulse and the relation of an output waveform for the example of a circuit to this figure (b) is shown in drawing 12 (a) at CCD, respectively. The datum point of a pulse is 0V and is the amplitude of +12V. A clock phi 5 and phi 6 The fields 17 and 18 under the given electrode express the last part of the level register 6. In addition, +5VDC is added to +12VDC and a substrate 48 to n-WERU 22 at +12VDC and the output gate (OG) 13 at +7VDC and the reset drain (RD) 16. Moreover, 15VDC and a source 9 are grounded by the drain 8 of MOSFET for amplification through load resistance. Therefore, this MOSFET is operating as a source follower circuit. Operation is hereafter explained using this figure (b).

[0010] It is assumed that a signal electric charge reads one after another, and is transmitted to a circuit by the level register 6. Now and time t1 It sets and is a clock pulse phi 5. Since it is high-level, it is a clock phi 5. The potential well is formed in the field 17 under the added electrode 7, and the signal electric charge is transmitted to the field 17. Next, time t2 Clock phi 5 A low level and phi 6 Since it becomes high-level, it is a clock phi 5. The potential well in the field 17 under the added electrode 7 disappears, and is a clock phi 6. A potential well is formed in the field 18 under the added electrode 7. Therefore, the above-mentioned signal electric charge is transmitted to a field 18. Time t3 Since it sets and a pulse is added to the reset gate (RG) 15, the potential of the floating diffusion (FD) 14 is reset by 12V which is the potential of RD16. Time t4 Since the signal electric charge has not been then transmitted to FD14 yet, potential is maintaining the reset value.

Time t5 It sets and is a clock phi 6. Since it is set to a low level, the signal electric charge which existed in the field 18 of the last part of the level register 6 overcomes the low potential barrier currently formed of low DC bias added to OG13, results in FD14, and changes the potential. Since an electron flows in so that it may understand also in the example of the output voltage of this figure (b), it is a clock phi 6. If set to a low level, an output will be extended toward the bottom. FD14 are connected with the gate of the source follower circuit (MOSFET) by wiring, and can obtain the output of the same size as having been inputted into the gate from the source by low impedance.

[0011] Thus, since the feature of a full frame transmission mode does not have an accumulation part and a large area of a light sensing portion can be taken, the capacity factor of light is widely used for the use of weak light, such as an object for Measurement Division, highly therefore. Since incidence light is absorbed with a transmission electrode on the other hand, the sensitivity fall to a blue light with a short wavelength is remarkable. As stated previously, although drawing 11 shows a typical light sensing portion, the PSG film 19 which the polysilicon electrode 20 covers the surface without a crevice, and amounts to several microns in thickness for separation of each electrode has piled it up. Since especially polysilicon absorbs the light and the electron of 400nm or less of a wavelength, it cannot be contributed to photoelectrical conversion.

[0012] About such an optical power detector, a substrate 48 is made thin to about 20 micrometers from 15 micrometers, and there is a thing it was made to irradiate light from the back as shown in drawing 13 . Although a photoelectrical conversion part will be prepared under gate oxide 21, the polysilicon electrode 20 will cover it without a crevice and short wavelength light will be absorbed, there is no obstacle other than the thin oxide film 23 in the back of a substrate 48, and high sensitivity can be expected to short wavelength light. This back irradiation type CCD has sensitivity to about 0.1nm short wavelength light, and is further applied also to an electron bombardment type CCD image pick-up device. Since this device can use a **** operation of the signal electric charge produced by electron bombardment, it is expected as a high sensitivity image pick-up device.

[0013] The example of representation of the manufacture process of back irradiation type CCD is explained here. First, it is P/P+ as UEFA. Type EPIUEFA is used. The specific resistance and thickness of this epilayer are 30 ohm-cm and 30 micrometers, respectively, and a substitute's specific resistance and thickness are 0.01 ohm-cm and 500 micrometers, respectively. All the CCD manufacture processes beforehand included to (Aluminum aluminum) wiring process are terminated to this EPIUEFA. Although giving aluminum wiring after the formation of a thin form of the light sensing portion silicon in a next process is naturally also considered, it is difficult to use the photograph etching method for the portion of the film formed into the thin form, and there is fear, like the portion formed into the thin form in the aluminum wiring process can be broken. For this reason, it is because it is necessary to end as many processes as possible before forming a thin form.

[0014] Next, the nitriding silicon and the oxide film which are attached to the UEFA back are removed.

[0015] Then, the chromium/gold layer which comes to laminate chromium and gold all over the back are deposited. And the portion which hits an acceptance surface, i.e., the field equivalent to a back entrance plane, removes chromium/gold layer.

[0016] Above-mentioned EPIUEFA is attached to a holder with wax after dividing into a chip. Then, HF:HNO3 : A silicon substrate is etched from the back using the etching solution of the rate of CH3 COOH=1:3:8, leaving the circumference part of a chip thickly. this etching solution -- nitric acid -- the dissolution according to fluoric acid since it is rich -- it is rate-limiting and etching progresses. here -- the

dissolution -- why rate-limiting etchant is used widely is explained. if -- fluoric acid -- if rich -- oxidization -- it is rate-limiting and etching progresses. UEFA used is P/P+. Since it is type, it is P+. If only a layer is etched alternatively, what was excellent in the homogeneity within the absolute value of film thickness and a field can be manufactured, and it will be very easy to perform the reproducibility of short wavelength sensitivity, and homogeneous control. P+ since the oxidization speed of a layer is quick -- oxidization -- if a rate-limiting etching solution is used, it will be easy to make the thing excellent in the homogeneity of film thickness, or reproducibility.

[0017] However, it is P+ actually. Many crystal defects are in a layer and a crystal defect is P+. Since oxidization speed is still quicker than a layer, it will be carried out quickly, and the crystal defect which suited in the middle of etching after all makes film thickness of an etching side uneven, and etching also results in dimming an acceptance surface. therefore, oxidization -- the dissolution which cannot use rate-limiting etchant and cannot perform control of film thickness easily -- rate-limiting etchant must be used. Moreover, if the thing of an alkali system is used as etchant, it excels in the ease of carrying out of homogeneous control of film thickness, but gate oxide is polluted with an alkaline metal and, unlike a design value, a MOS device like CCD causes a defect of operation for threshold voltage etc. Therefore, in the process, etchant of an alkali system was not used conventionally.

[0018] Next, film thickness is measured. As a result, when film thickness is inadequate as a desired value, it etches again.

[0019] Next, back oxidization is performed for above-mentioned UEFA in 120-degree-C steam for 48 hours. Since it has already ended to aluminum wiring, it is impossible to add high temperature and to oxidize. For this reason, prolonged oxidization is performed at the low temperature of 120 degrees C.

[0020] Next, what is called back AKYUMURESHON that irradiates negative ion is performed to a back oxide film. As mentioned above, as for back irradiation type CCD, the back of CCD turns into an entrance plane of light. Usually, the thickness of silicon UEFA which forms CCD is hundreds of microns. Moreover, 200 to 300nm light will have a very large absorption index, and will be absorbed in the place into which the most went slightly from the surface. Therefore, even if it uses CCD which has a thickness of hundreds of microns as a back irradiation type as it is, the photoelectron generated with the back cannot be diffused to the potential well of CCD in the surface, but it will re-join together and most will be lost. Moreover, even if some of them are able to reach to a potential well, while diffusing a long distance, signals are mixed and they reduce what is called resolution remarkably. Therefore, the back which is an acceptance surface is made thin by etching and polish, and the generated electron must enable it to arrive at a surface potential well by the shortest distance at back irradiation type CCD.

[0021] The thickness of the detection element by typical silicon as shown in drawing 13 is 10-15 micrometers. An oxide film 23 is hundreds of A from 10A of thickness numbers here.

[0022] Drawing 14 shows the potential profile of the section of a to [from an acceptance surface / surface CCD] about the silicon detection element formed into the thin form in drawing 13 . Toward Drawings, left-hand side expresses the back and right-hand side expresses the surface. In addition, a substrate 48 is P type. The oxide film 23 which is a protective film has grown to be the back of a substrate 48.

[0023] However, an oxide film electric charge and interface semi- grade certainly exist in an oxide film 23, and each of these works so that the surface of P type silicon substrate 48 may be made to ****-ize. Namely, the potential to an electron becomes low as the solid line in drawing 14 showed and the oxide film 23 on the back will be approached, if it sees by a potential profile. That is, the photoelectron produced from the back in

the shallow place cannot go to the potential well of CCD, but serves as fate which waits to be pushed aside and to re-combine with the interface of the back oxide film 23 and silicon. Therefore, by irradiating the ion which formed the light sensing portion into the thin form, and was charged in negative after oxidizing the back, the surface of P type silicon 48 near the back oxide film 23 is changed into an AKYUMURESHON state, and it is made a potential profile as shown in the dotted line in drawing 14 . The photoelectron which this produced in the shallow place of the back can also arrive at the potential well of CCD by the side of the surface efficiently.

[0024] In addition, although what is necessary is just to carry out the ion implantation of the boron to P type silicon substrate when performing AKYUMURESHON generally, the ion implantation layer must become amorphous [-like] and must activate the boron atom which carried out ion implantation to re-crystallization by subsequent heat treatment. Usually, this heat treatment (annealing) needs to perform what is called a 2 step annealing that performs heat treatment near 600 degree C and near 1000 degree C continuously. It becomes the source of leak current and is not desirable if an annealing runs short. However, since aluminum wiring is already given, such a hot annealing cannot be performed. Therefore, as for AKYUMURESHON of the back silicon by ion implantation, it is actual to have adopted only negative AKYUMURESHON of being unable to do but irradiating negative ion.

[0025] Finally UEFA which passed through above-mentioned operation is mounted in a package. It is technology important when measuring weak light to cool CCD and to lower leak current and a rms noise. Therefore, in this process, heat resistance pastes up the surface of the silicon substrate formed into the thin form, i.e., the field in which CCD is formed, on a package through resin of small non-conducting etc.

[0026]

[Problem to be solved by the invention] However, a problem is in the durability of an effect, in order to raise the sensitivity of short wavelength light, having performed such work is not concerned, either, but above AKYUMURESHON becomes that the negative ion conversely attached to the back oxide film by irradiation of short wavelength light removes, and is easy to be neutralized. That is, the state, AKYUMURESHON, will be in a **** state again, and there is a problem that the sensitivity to short wavelength light will be lost.

[0027] Moreover, also in the process which manufactures an above-mentioned detector, it has some problems. for example, etching of a substrate -- the dissolution -- in order to use rate-limiting etchant, film thickness will become remarkably uneven, if an etching solution is fully agitated and always new etchant is not supplied to an etching side. However, however it may agitate, film thickness becomes uneven easily by surroundings lump of etchant etc. at the boundary part of an etching portion and the portion which is not etched. Furthermore, when measuring film thickness, you have to remove CCD once from a holder. However, there is a possibility that it may damage a thin film part in the midst of taking from subSUTOREITO or sticking the portion which is already equivalent to the light sensing portion of CCD since film thickness is quite thin.

[0028] In order to oxidize at low temperature in the process of back oxidization, the character of an oxide film is not so good and a possibility that many traps will work as a source of leak current is high.

[0029] In a mounting process, when silicon with a thickness of 10 to 15 micrometers formed into the thin form is made to attach and harden resin afterwards, compression stress may arise at the time of hardening of resin, and it will be concentrated and waved by the power in a thin film part, and may result in breakage of a crack etc.

[0030] As stated above, the conventional back irradiation type CCD has problems also including the process

which obtains the composition. That is, about a substrate, when performing aluminum wiring after the formation of a thin form, the flexibility of AKYUMURESHON on the back becomes large, and ion implantation and 2 step annealing can be performed. However, the photograph etching method at the time of aluminum wiring is difficult, and, moreover, there is a possibility that a thin film part may be damaged, at the time of hardening of DAIBONDO resin. That is, the yield is quite low although a thing with this sufficient method in characteristic is obtained.

[0031] On the other hand, since it is only performing an assembly after the formation of a thin form when performing thin form-ization after aluminum wiring, the probability that a thin film part will be damaged becomes small. However, the problem that leak current will be large even if back AKYUMURESHON is difficult and is made, and the variation per hour of sensitivity is moreover large arises. Moreover, there is a possibility that a thin film part may be damaged, at the time of hardening of DAIBONDO resin. That is, although this method is not bad in yield, there is a problem very much in characteristic.

[0032] Then, this invention aims at offering the semiconductor energy detector which solved the above-mentioned problem.

[0033]

[Means for solving problem] [the semiconductor energy detector of this invention / the surface of the semiconductor thin board which has the 1st conducted type of current] In the semiconductor energy detector which detects the energy of the electromagnetic waves which the electric charge read-out part which has-dimensional [1] or two-dimensional arrangement is formed, and enter from the back to the formation side of the electric charge read-out part of a semiconductor thin board, or a charged particle The semiconductor layer which consists of a semiconducting material which has a bigger band gap than the band gap which has the 1st conducted type of current, and the composition material of a semiconductor thin board has is formed in the back of a semiconductor thin board. The formation material of a semiconductor thin board and the formation material of a semiconductor layer are material of the same kind, and it is characterized by being good also as a feature and the semiconductor thin board and the semiconductor layer carrying out hetero combination of the crystal structure being different. Here, it is good also considering the formation material of a semiconductor thin board and the formation material of a semiconductor layer being material of a different kind as a feature. Moreover, it is good also considering photoelectrical conversion being formed in the thickness which is not performed substantially inside a semiconductor layer as a feature.

[0034] [moreover, the manufacture method of the semiconductor energy detector of this invention] (a) The 1st process which forms the electric charge read-out part which has-dimensional [1] or two-dimensional arrangement in the surface of the semiconductor board which has the 1st conducted type of current, (b) Process the back of the semiconductor board to the formation side of an electric charge read-out part. [a semiconductor board / the 2nd process used as a semiconductor thin board, and the back of (c) semiconductor thin board] While having a bigger band gap than the band gap which has the 1st conducted type of current, and the composition material of a semiconductor thin board has, it is characterized by including the 3rd process which deposits the semiconducting material which carries out a hetero-junction to the composition material of a semiconductor thin board, and a semiconductor layer forms. Here, it is good also considering forming a semiconductor layer with a CVD method as a feature.

[0035]

[Function] It has the conducted type same according to the semiconductor energy detector of this invention as the conducted type of current which a semiconductor thin board has of current. And the semiconductor

layer which consists of a semiconducting material which has the bigger energy between semi- grades than the energy between semi- grades which a semiconductor thin board has carries out a hetero-junction, and is formed in the back side of the semiconductor thin film into which an energy line enters. For this reason, the potential to the signal electric charge by the side of the entrance plane of this detector becomes high, the diffusion to the direction of an energy line entrance plane is controlled, and the signal electric charge produced with the incidence energy line realizes the AKYUMURESHON state which accumulates an electronic group effectively. The amount of electric charges which reflected the amount of energy of the incidence energy line faithfully can be transmitted in read-out of an accumulation electric charge, and the semiconductor energy detector whose sensitivity and accuracy over an energy line improved can be obtained.

[0036] Moreover, according to the manufacture method of the semiconductor energy detector of this invention, an electric charge read-out part is first formed in one surface of a semiconductor board. Next, the surface (it is hereafter called the back) of another side is ground or etched, and a semiconductor board is thin-board-ized. Subsequently, have the same conducted type as a semiconductor thin film of current in the back side, and a semiconducting material with a bigger band gap of an energy level than a semiconductor thin film is made to deposit, and a semiconductor layer is formed. Therefore, by performing [CVD method] the semiconducting material of a wide band gap in a low-temperature process comparatively It is possible to make it deposit below in the melting point of aluminum, and it is not necessary to cause melting of the aluminum wiring given in the electric charge read-out part and modification which were given before this deposition process. Moreover, since necessities, such as low-temperature oxidization, are lost, a semiconductor energy detector can be manufactured without worries about the corrosion of the above-mentioned aluminum wiring.

[0037]

[Working example] The work example of the semiconductor energy detector concerning this invention is hereafter explained using a figure.

[0038] Drawing 1 shows the sectional view of the semiconductor energy detector concerning the work example of this invention. As shown in this figure, on silicon UEFA 35 currently fixed to the bottom in a package 38, P type silicon layer 48 as a P type silicon thin board which has CCD31 is installed through the metal bump 32 in the field which counters the silicon UEFA 35. The wide band gap layer 24 which consists of P type amorphous silicone carbide (it is henceforth called P type a-silicon carbide) is formed in the field which has not countered silicon UEFA 35 of this P type silicon layer 48.

[0039] In an above-mentioned back irradiation type semiconductor energy detector, the wide band gap layer 24 which carries out a hetero-junction to P type silicon layer 48 at the acceptance surface side of P type silicon layer 48, and consists of P type a-silicon carbide with a larger band gap than P type silicon layer 48 is formed. Thereby, the AKYUMURESHON state is maintained. Therefore, the sensitivity to short wavelength light serves as a detector which is moreover stable uniformly within the same chip.

[0040] Drawing 2 shows the structure of the light sensing portion of this semiconductor energy detector. Although the structure shown in this figure is similar to the structure of the light sensing portion of the conventional semiconductor energy detector shown in drawing 13 and is in sight The wide band gap layer 24 formed in the acceptance surface side of P type silicon layer 48 is a semiconductor layer which consists of P type a-silicon carbide, and while differing in that the hetero-junction is carried out, effects differ notably about discovery of an AKYUMURESHON state.

[0041] Drawing 3 shows the situation of the hetero-junction with the wide band gap layer 24 which consists of an above-mentioned P type silicon layer 48 and P type a-silicon carbide. Drawing 3 (a) shows the band structure inside P type silicon and P type a-silicon carbide. In addition, a numerical unit is eV and the value about P type a-silicon carbide may change a little with processes.

[0042] It is the semiconductor with which a-silicon carbide has an about 2eV band gap to the band gap of silicon being 1.1eV. Moreover, to the grating constant of silicon being about 54.3nm, a-silicon carbide is about 43.6nm (it changes a little with processes) grating constant, and is a little narrow. In addition, the electron affinity of silicon and the electron affinity of a-silicon carbide are comparable.

[0043] If the semiconductor with which such band gaps differ is contacted, in an equilibrium situation, an interaction will arise according to an interface so that a Fermi level may become fixed. That is, an electron moves to P type silicon from P type a-silicon carbide, an electron hole moves to this opposite direction, and an equilibrium situation is attained when a Fermi level gathers. Therefore, the band structure when contacting these two semiconductors becomes as it is shown in drawing 3 (b). In near a contact surface, a band becomes discontinuous because [of lattice mismatching], and since the difference of the grating constant of silicon and a-silicon carbide is comparatively great, it is thought that much interface semi- grade will exist near a contact surface.

[0044] If the conducting zone near the contact surface in an equilibrium situation like drawing 3 (b) is seen, since the minimum energy value of a conducting zone will descend in a-silicon carbide field, on this figure, a band bends downward, and since the minimum energy value of a conducting zone rises in a silicon field, on this figure, a band bends upward. Therefore, if the layer which becomes the entrance plane of back irradiation type CCD from a-silicon carbide is formed, a hetero-junction will be formed of the difference of a band gap, and a very desirable AKYUMURESHON state will be realized for P type silicon near a contact surface.

[0045] drawing 4 -- P type silicon thin film 48 from the wide band gap layer 24 (all over a figure, it is only described as P-SiC) -- the CCD potential well 3 is reached further -- until is expressed as a potential figure for an electron. Drawing 4 (a) makes an incidence energy line light, and the case where the wide band gap layer 24 is comparatively thick (about tens of micrometers or more) is shown. In this case, a comparatively short light of about 600nm or less is absorbed in the field of the wide band gap layer 24, and photoelectrical conversion of the wavelength is carried out. If a neutral field is large within the wide band gap layer 24, the electronic group by which photoelectrical conversion was carried out will wander about the inside of a neutral field, among those will carry out **** combination. By chance, only the signal electric charge which reached the contact surface will flow into P type silicon thin film 48 and also the CCD potential well 3 according to potential inclination, and will be read by spreading diffusion as a signal. That is, if the wide band gap layer 24 is so thick that a neutral field becomes large, short wavelength sensitivity will fall. A neutral field does not appear or the thickness of the wide band gap layer 24 to which a neutral field becomes narrow enough is about tens of micrometers or less. the signal electric charge which the inside of the wide band gap layer 24 changed into the state where **** was mostly added over the whole region, and was generated when it was this -- almost -- all -- P type silicon thin film 48 -- it flows into the CCD potential well 3 further, and is read as a signal, and sensitivity becomes good also to short wavelength light by **. Although it said that the comparatively big difference of the grating constant of silicon and a-silicon carbide generates much interface semi- grade previously, a contact surface is the strongest portion of ****, and since a signal electric charge can pass at high speed, the probability that a signal electric charge will be captured at interface semi- grade

is small.
[0046] Furthermore, in order to improve sensitivity, as shown in drawing 5 , the wide band gap layer 24 is formed in a thickness of about thousands of [hundreds to] nm. It can be used only in order to bend the band of P type silicon layer near a contact surface, and it can also be considered as the structure which photoelectrical conversion does not generate in the wide band gap layer 24 substantially. Since such structure, then the wide band gap layer 24 are very thin, not to mention long wavelength light, short wavelength light also almost penetrates the wide band gap layer 24, is absorbed in P type silicon layer 48, and performs photoelectrical conversion. Although short wavelength light carries out photoelectrical conversion near a contact surface and a signal electric charge is produced, since it is in the AKYUMURESHON state where it is good near a contact surface, as [show / in drawing 5], the electronic group which is the generated signal electric charge flows into the CCD potential well 3 efficiently. Therefore, the sensitivity to short wavelength light can be improved by leaps and bounds.
[0047] Next, the manufacture method of the semiconductor energy detector concerning an above-mentioned work example is explained using a figure.
[0048] First, P/P+ which is start material P type silicon layer 48 is obtained by type single crystal epitaxial growth (drawing 6 (a)). This P type silicon layer 48 is 30 micrometers in specific resistance 30 ohm-cm and thickness, for example, and subSUTOREITO is 500 micrometers in specific resistance 0.01 ohm-cm and thickness, for example.
[0049] Next, the surface of P type silicon layer 48 is processed. This figure (b) forms CCD31 in the upper surface of P type silicon layer 48, and shows the state where metal wiring 30 was given further.
[0050] Subsequently, the silicon nitriding film 33 is deposited on the whole surface of the surface of P type silicon layer 48 and the back which ended the process to this figure (b). Then, the silicon nitriding film 33 of the field you are on the field in which CCD31 are formed, and the metal bump 32 wants to grow up to be is removed. Moreover, in respect of being opposite to the field in which CCD31 were formed, the silicon nitriding film of a portion to thin-shape-ize is removed.
[0051] The example which forms a solder bump with an supersonic method is shown as the metal bump's 32 formation method here.
[0052] Drawing 7 is the schematic view of ultrasonic soldering equipment. The jet stream of the solder 43 which fills the inside of the solder tub 45 is done by the churning child 44 currently installed in the inside of the solder tub 45. CCD UEFA 41 is perpendicularly arranged in the solder 43 which is carrying out the jet stream, and the ultrasonic transducer 42 is put on the upper part of this solder tub 45 so that the vertical plane of that CCD UEFA 41 may be countered from the exterior of the solder tub 45. Always fresh solder is sent to the field of CCD UEFA 41 which counters the ultrasonic transducer 42 with this equipment, and it is the solder tub 45N2. Oxidization of solder is prevented by making it flow.
[0053] Next, the mechanism of ultrasonic soldering using above-mentioned equipment is explained. First, if KYABITEI arises in solder 43 in an operation of an ultrasonic wave and this KYABITEI **** on the surface of CCD UEFA 41, the natural oxidation film on aluminum electrode currently formed in UEFA 41 will be destroyed. If this natural oxidation film is removed, a eutectic crystal reaction will occur between aluminum electrodes currently formed, and a bump will be formed. Since a eutectic crystal reaction does not occur in the portion which are not metal, such as a PASSHIBESHON film, there is no adhesion of solder in it. Therefore, although a part of field of 33 silicon nitriding film opposite to the side in which there is no growth of solder in the portion in which the silicon nitriding film 33 is formed, and CCD31 are formed cannot be found,

since 48 layers of P type silicon which the thin natural nitriding film attached there exists, there is no growth of solder too.

[0054] The solder bump 32 shown in drawing 6 (c) is formed by an above-mentioned method. Although a bump tens of microns high is formed to 100-micron square aluminum pattern in an supersonic method, since a bump's height formed can also be made high, the adjustment is so possible that the film thickness of aluminum of a ground is thick. Moreover, as a bump's method of forming, there are also a vapor-depositing method and the other plating methods, and a bump's height formed also by those methods can be changed.

[0055] Finally it is divided into each chip by dicing etc. This will be in the state of drawing 6 (c).

[0056] SubSUTOREITO is prepared apart from the above procedure. Drawing 8 (a) shows subSUTOREITO for supporting a CCD chip, and its glass with equal silicon UEFA or CCD chip, and coefficient of thermal expansion is desirable. Here, the time of using silicon UEFA 35 as subSUTOREITO is explained. First, silicon UEFA 35 is oxidized, the oxide film 37 of suitable thickness is formed, and metal wiring 34 of aluminum etc. is given. This metal wiring 34 connects the electrode of a package to the metal bump 32 who formed on the CCD chip indirectly. Then, since the portion which touches etchant of silicon is guarded, the silicon nitriding film 36 is deposited on both sides, and a CCD chip removes the field compared by silicon UEFA 35 by etching at a next process. What is shown in drawing 6 (c) and drawing 8 (a) is made into one after an appropriate time.

[0057] Drawing 8 (b) shows the state where bump bonding of silicon UEFA 35 which gave metal wiring 34 was carried out to the CCD chip in which the above-mentioned metal bump 32 was formed. The side in which CCD31 are formed compares and it has become a field so that it may be illustrated. Moreover, it is filled up with resin 50 so that etchant of the silicon behind used for the compared field in this figure may not enter. This resin 50 is the Nippon Kayaku make, for example. Kaya TRON It is ML-230P. Heat treatment performs hardening of resin 50. As mentioned above, almost all resin produces compression stress at the time of hardening, but since a CCD light sensing portion is before still forming it into a thin form, the whole CCD chip distributes, after the formation of a thin form, it is cracked to an acceptance surface or compression stress does not break. In addition, the etchant used in a next process is borne [that the feature needed for resin 50 is non-conducting,], It is an alkaline metal's etc. not being included, contraction stress suitable at the time of hardening working, and keeping contact of a bump bonding area good, and bearing the about 150-degree C heat at the time of DAIBONDO or a wire bond.

[0058] Then, 8 regulation KOH:H2 O:isopropyl alcohol = a silicon substrate is etched from the back using alkali system etchant, such as 950ml : 1150ml : 700 etc.ml, leaving the circumference part of a chip thickly (drawing 8 (c)). Here, it is HF:HNO3 as etchant. : You may use the etching solution of the rate of CH3 COOH=1:3:8. this etching solution -- nitric acid -- the dissolution according to fluoric acid since it is rich -- it is rate-limiting and etching progresses. It is important for etching to stop in the state where P type silicon layer 48 is not penetrated. If composition and temperature of etchant are constant, an etching rate will not change, therefore if film thickness is measured in the middle of 2 to 3 times etching, etching can be ended in the meant place.

[0059] In this example, etchant is heated at 78 degrees C, using alkali etchant, the CCD chip by which bump bonding was carried out to silicon UEFA 35 is rotated so that it may self-revolve around the sun, and the bubble generated in an etching side is removed. When removal of a bubble is inadequate, it is because there is uneven ******** possibility of the roughness of an etching side or film thickness. As for an etching rate, a part for about 0.6-micrometer/is obtained.

[0060] the dissolution which lessened quantity of fluoric acid since an acceptance surface was not dimmed according to a crystal defect in the case of acid etchant of a hydrofluoric-and-nitric-acid system -- although rate-limiting etching is used -- the dissolution -- as for rate-limiting etchant, film thickness becomes uneven easily. However, in alkali system etchant, since anisotropic etching is possible, film thickness becomes uniform.

[0061] Since CCD of this example is the device of a MOS system, naturally silicon UEFA of a plane direction <100> is used. Alkali system etchant has the hundreds-time-slower etching rate of <111> sides compared with <110> sides or <100>, when KOH is included, for example, therefore since etching will progress along <100> sides if it is clear and carries out so that a bubble etc. may not reach an etching side, film thickness becomes uniform.

[0062] The surface silicon nitriding film 33 is removed after the end of silicon etching. Then, as shown in this figure (d), the P type a-silicon carbide which is a wide band gap semiconducting material is made to deposit with a CVD method etc., and the wide band gap layer 24 is formed in an acceptance surface. Here, if an optical CVD method is used, low-temperature-izing is still more possible.

[0063] Drawing 9 includes back irradiation type CCD formed by the above-mentioned method in the packages 38, such as ceramics, and shows the state where between packages 38 was connected with silicon UEFA 35 by bonding 39. In addition, in X ray detection, elementary particle detection, etc., the window material 40 is unnecessary.

[0064] This invention is not limited to the above-mentioned work example, and various modification is possible for it. For example, as a material of a wide band gap layer, you may use P type amorphous silicone, a diamond thin film, cadmium TERURU, HI-ized gallium, cesium iodide, etc. in addition to the above-mentioned P type a-silicon carbide. Moreover, although the P type conducted type semiconductor of current was used in the above-mentioned work example, you may use the N type conducted type semiconductor of current.

[0065]

[Effect of the Invention] As explained to details above, according to the semiconductor energy detector of this invention, the semiconductor layer of a wide band gap is prepared in the back of a semiconductor thin board, and forms the hetero-junction. This wide band gap layer has the high potential to a signal electric charge compared with a semiconductor thin board, and realizes a good AKYUMURESHON state. Therefore, the signal electric charge generated by incidence of light etc. can be read efficiently. Moreover, dark current does not increase by charge rise. Moreover, a wide band gap layer does not serve as a source of generation of dark current, also when it is stable and uses it in a comparatively hot environment to temperature. Therefore, the semiconductor energy detector whose sensitivity to an energy line improved and was stable can be obtained.

[0066] Moreover, according to the manufacture method of this invention, AKYUMURESHON processing can be performed at low temperature after metal wiring, prolonged low-temperature oxidization etc. becomes unnecessary and the highly sensitive stable semiconductor energy detector can be manufactured in an easy process.

[Brief Description of the Drawings]

[Drawing 1] It is the schematic view showing the cross-sectional structure of the work example concerning this invention.

[Drawing 2] It is the figure showing the back irradiation type detector of the work example concerning this invention.

[Drawing 3] It is the explanatory view of the hetero-junction of the work example concerning this invention.

[Drawing 4] It is the figure showing the potential profile of the back irradiation type detector of the work example concerning this invention.

[Drawing 5] It is the figure showing the potential profile of the back irradiation type detector of the work example concerning this invention.

[Drawing 6] It is the manufacturing process figure of the semiconductor energy detector concerning this invention.

[Drawing 7] It is the figure showing the equipment for forming a metal bump.

[Drawing 8] It is the manufacturing process figure of the semiconductor energy detector concerning this invention.

[Drawing 9] It is the manufacturing process figure of the semiconductor energy detector concerning this invention.

[Drawing 10] It is the upper surface figure showing the composition of a full frame transmission mode.

[Drawing 11] It is the sectional view showing the important section of a full frame transmission mode.

[Drawing 12] It is the figure showing a read-out circuit diagram and a clock pulse output waveform.

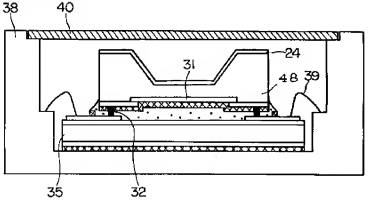
[Drawing 13] It is the figure showing the conventional back irradiation type detector.

[Drawing 14] It is the figure showing the potential profile of the conventional back irradiation type detector.

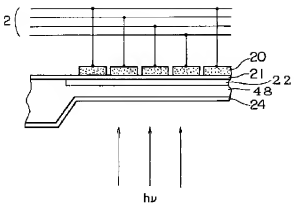
[Explanations of letters or numerals]

22 [-- CCD, 32 / -- A metal bump, 38 / -- A package, 40 / -- Window material, 48 / -- P type silicon layer.] -- n-WERU, 24 -- A wide band gap layer, 35 -- Silicon UEFA, 31

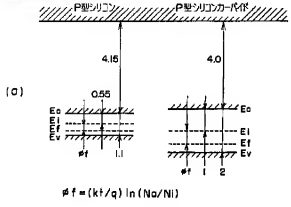
[Drawing 1]

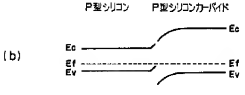


[Drawing 2]

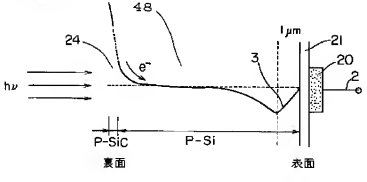


[Drawing 3]

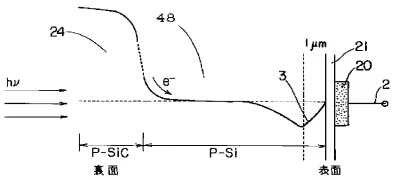




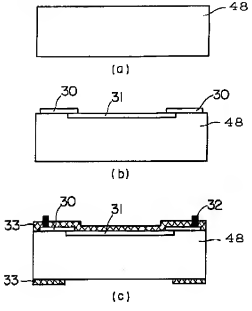
[Drawing 5]



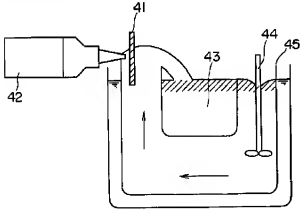
[Drawing 4]



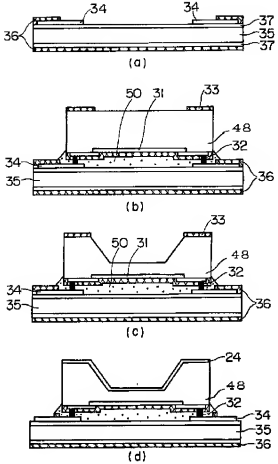
[Drawing 6]



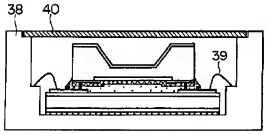
[Drawing 7]



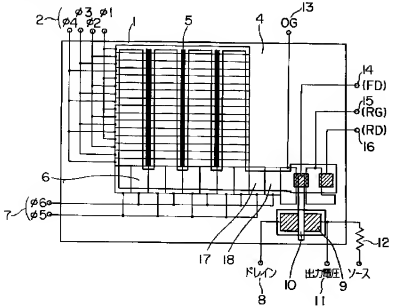
[Drawing 8]



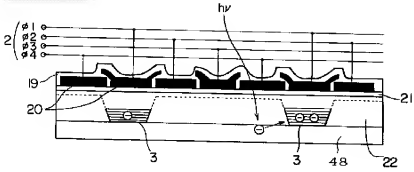
[Drawing 9]



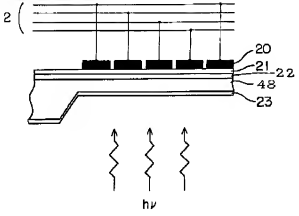
[Drawing 10]



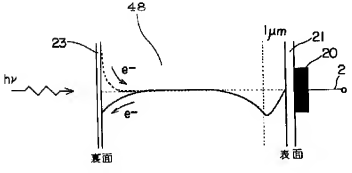
[Drawing 11]



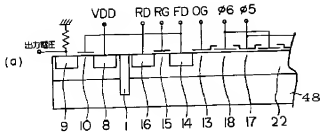
[Drawing 13]

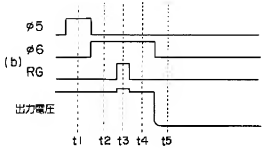


[Drawing 14]



[Drawing 12]





[Translation done.]